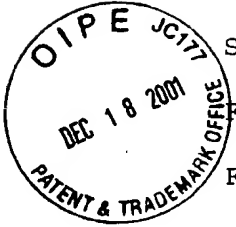


## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Applicants: YOSHIDA et al.

Serial No.: 09/416,959

Filed: October 13, 1999

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE  
AND PROCESS FOR MANUFACTURING THE SAME

Group: 2812

Examiner: R. Pompey

#8/D  
1/9/02  
V. Varnall  
RECEIVED  
DEC 21 2001  
162800 MAIL ROOM

PRELIMINARY AMENDMENTAssistant Commissioner for Patents  
Washington, D.C. 20231

December 18, 2001

Sir:

Prior to examination, please amend the above-identified  
application as follows.

IN THE CLAIMS

Please cancel claims 1-17 without prejudice or disclaimer  
of the subject matter thereof.

Please add new claims 18-41 as follows:

-- 18. A semiconductor integrated circuit device having a  
first portion for a memory array and a second portion for a  
circuit other than the memory array comprising:

first MISFETs arranged in said first portion, said  
first MISFETs each having a gate electrode and a source and a  
drain region;

D!  
Cmt